L&L-I0026

RAKE RECEIVER FOR OPERATING IN FDD AND TDD MODES

Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE02/01095, filed March 25, 2002, which designated the United States and was not published in English.

Background of the Invention:

Field of the Invention:

The invention relates to a RAKE receiver for reception of spread-coded signals in the FDD and TDD modes.

In the universal mobile telecommunications system (UMTS) standard for the third mobile radio generation, the frequency division duplex (FDD) mode is provided for the so-called "unpaired band" (which has separate frequency bands for the uplink and downlink directions) and the time division duplex (TDD) mode is provided for the "paired band" which uses a common frequency band for the uplink and downlink directions.

Owing to the widely differing spreading factors in these two modes (while the maximum spreading factor in the TDD mode is equal to 16, spreading factors up to 512 can be used in the FDD mode), it is necessary to use different receiver types and

different equalizer algorithms in order on the one hand to ensure as low a level of signal processing complexity as possible in the FDD mode, and on the other hand to make it possible to provide a given quality of service (QoS) in the TDD mode.

In multimode mobile radio receivers, it is therefore generally necessary to implement a RAKE receiver with matched filter (MF) equalization for the FDD mode and a multiple subscriber receiver with joint detection (JD) equalization for the TDD mode.

RAKE receivers and multiple subscriber receivers are fundamentally different receiver concepts. RAKE receivers are based on the principle that the signal interference caused by multipath propagation can be suppressed by detecting the individual signal versions which are received via the various propagation paths, and then by joining the signal version together with the correct timing. Multiple subscriber detection is based on the idea of eliminating interference caused by other active mobile radio subscribers (so-called intracell interference) by explicit detection of the subscriber signals, that is to say making use of the fact that the interference caused by the activities of other subscribers is deterministic (not random noises).

The implementation of two different receiver structures in multimode mobile radio receivers has a disadvantageous effect on the production costs and, furthermore, has a disadvantageous effect on technical parameters such as power consumption. It is thus desirable to provide a common receiver structure, which is suitable for operation both in the FDD mode and in the TDD mode.

Summary of the Invention:

It is accordingly an object of the invention to provide a RAKE receiver for operating in the FDD and TDD modes that overcomes the above-mentioned disadvantages of the prior art devices of this general type, which allows reception operation both in the FDD mode and in the TDD mode. A further aim of the invention is to provide a reception method that allows multimode FDD and TDD operation in a manner that is as simple as possible.

With the foregoing and other objects in view there is provided, in accordance with the invention, a RAKE receiver for receiving signals transmitted by different propagation paths of a transmission channel and spread-coded with chip sequences in frequency division duplex and time division duplex modes. The rake receiver contains at least two RAKE fingers, an equalizer connected to the RAKE fingers for equalization of the signals processed in individual ones of

the RAKE fingers using equalizer coefficients, and a calculation unit for generating the equalizer coefficients for the FDD and TDD modes selectively. The equalizer coefficients for the TDD mode being calculated using a multiple subscriber method on a propagation path non-specific basis for each chip of the signals to be equalized, and being applied to the signals. The calculation unit is connected to the equalizer.

The receiver structure according to the invention is accordingly a RAKE receiver that has two or more RAKE fingers in the normal way. The RAKE fingers have an associated equalizer, using which the signals that are processed in the individual RAKE fingers are equalized using equalizer coefficients. The equalizer according to the invention has a unit for calculating the equalizer coefficients for the FDD and TDD modes selectively, for example on the basis of channel estimation. According to the invention, the equalizer coefficients for the TDD mode are in this case calculated using a multiple subscriber calculation method for each chip of the signals to be equalized, and are applied to the signals.

The invention is based on the knowledge that the RAKE receiver structure which has been used until now for individual subscriber detection on the basis of MF equalization can also be used for multiple subscriber detection (which is absolutely

essential in the TDD mode), provided that equalizer coefficients are calculated - in contrast to the situation in the FDD mode - per chip, and are applied by the equalizer to the signals in the RAKE fingers. As will be explained in more detail in the following text, this makes it possible to carry out JD equalization by a RAKE structure that has only minor physical changes in comparison to a conventional RAKE receiver.

One advantageous exemplary embodiment of the invention is characterized in that a unit for signal rate reduction, in particular an accumulator, is provided in the signal path upstream of the equalizer in each RAKE finger, and in that a device is further provided for bridging the unit for signal rate reduction. The device for bridging the unit for signal rate reduction results in that the signal rate at the input of the equalizer can selectively be set to the symbol rate (which is required, for example, for MF equalization in the FDD mode) or to the chip rate (which is required for JD or multiple subscriber equalization in the TDD mode).

A further advantageous refinement of the RAKE receiver according to the invention is characterized in that a combiner is provided in the signal path downstream of the equalizer and accumulates output signals from RAKE fingers which are associated with the same physical channel, and in that the

combiner is configured to carry out signal rate reduction from the chip rate to the symbol rate in the TDD mode. Therefore, the combiner additionally acts as an integrate and dump unit in the TDD mode, which accumulates the weighted chips which are emitted from the equalizer over one symbol time period and, as a consequence of this, converts the signal rate from the chip rate to the symbol rate.

A further advantageous embodiment variant of the RAKE receiver according to the invention is characterized in that a multiplexer is connected upstream of the equalizer (which is, in particular, in the form of a multiplication field), and a demultiplexer is connected downstream of it. The multiplexing of the equalizer that two or more RAKE fingers can be associated with a single function element (multiplier) of the equalizer.

The device for calculating the equalizer coefficients preferably carries out a zero forcing (ZF) calculation for determination of the equalizer coefficients in the TDD mode. ZF equalization is a simple JD equalization algorithm for calculation of the equalizer coefficients.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a RAKE receiver for operating in the FDD and TDD modes, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a simplified block diagram for explaining the structure of a baseband section of a RAKE receiver according to the invention;

Fig. 2 is a block diagram of a rake finger section and a combiner, as illustrated in Fig. 1, in greater detail;

Fig. 3 is a block diagram of the combiner, as illustrated in Fig. 2, in greater detail; and

Fig. 4 is an illustration for explaining joint detection equalization using a RAKE receiver.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a baseband section of a RAKE receiver according to the invention that has an input memory IN_RAM to which a signal containing a stream of complex data $\underline{r}$ is supplied. The input memory IN_RAM provides buffer storage for the data $\underline{r}$.

The baseband data $\underline{r}$ is produced in the normal way, for example by a non-illustrated heterodyne stage. This contains, for example, a radio-frequency mixing stage which produces analog in-phase (I) and quadrature (Q) signal components from a signal received via an antenna, and down-mixes the signal components by frequency mixing to a suitable intermediate frequency or to a baseband. The down-mixed analog I and Q signal components are digitized by analog/digital converters. Digitization is carried out, for example, using a sampling rate of $2/T_c$, where T_c is the chip time period of the received data signal. The individual chips of the spreading codes which are used for CDMA multiple access can thus be separated (in UMTS mobile radio systems, the chip time period is T_c = 0.26 µs, that is to say a sampling rate of $2/T_c$ corresponds to approximately 8 MHz).

The digitized I and Q signal components are then smoothed in a likewise known manner, by a digital low-pass filter and, if necessary, their frequencies are corrected by a frequency correction unit.

A search and synchronization unit SE accesses the data $\underline{r}$ stored in the input memory IN_RAM and, on the basis of an evaluation of pilot symbols contained in this data or pilot symbols which have already been separated from the data signal, identifies the data structure of different signal versions which are received via different propagation paths, and identifies the timings of the signal versions.

Path information ADD_P determined by the search and synchronization unit SE and relating to the occurrence and number of different signal versions is passed to the input memory IN_RAM, and synchronization information Sync is supplied to a RAKE finger section RF of the RAKE receiver.

The RAKE finger section RF contains two or more RAKE fingers. The data $\underline{r}$ is distributed between different RAKE fingers by use of the path information ADD_P in a manner that will be explained in more detail later. The synchronization information Sync results in the data being synchronized in the RAKE fingers.

A weighting unit WG is disposed within the RAKE finger section RF, is formed from a hardware multiplication field and weights the signals in the individual RAKE fingers. The weighting unit WG is supplied with equalizer coefficients that are calculated by a calculation unit CU.

Output signals from the individual RAKE fingers are produced at the output of the RAKE finger section RF. These output signals are supplied to a combiner CB (for example a Maximum Ratio Combiner) in accordance with the normal configuration of a RAKE receiver. The combiner CB adds those signal versions that are processed in the individual RAKE fingers and are associated with a single physical channel, and emits a stream of estimated data symbols $\hat{\underline{s}}$. That is to say, $\hat{\underline{s}}$ denotes the reconstructions, as determined at the receiver end, of the data symbols $\underline{s}$ transmitted from a transmitter.

The baseband section of the RAKE receiver, as illustrated in Fig. 1, also has a channel estimator CE that determines discrete impulse responses for the received physical channel or channels and for their different transmission paths.

The discrete-time impulse responses determined by the channel estimator CE are passed to the calculation unit CU, in order

to calculate equalizer coefficients. The calculation unit CU calculates the equalizer coefficients as a function of the operating mode (FDD or TDD) that is intended to be carried out by the RAKE receiver. The desired operating mode is set via a selection switch SEL. The selected operating mode is signaled not only to the calculation unit CU but also to the RAKE finger section RF and to the combiner CB.

The spreading codes C_{SP} and scrambling codes C_{SC} that are available in the mobile radio system are stored in a code memory CDS. The code elements of these codes are referred to as chips. The codes are available not only for the calculation unit CU for calculation of the equalizer coefficients, but also for the RAKE finger section RF of the RAKE receiver.

Fig. 2 shows the RAKE finger section RF, as illustrated in Fig. 1, and the combiner CB in greater detail.

As can be seen from Fig. 2, the RAKE finger section RF has, for example, eight (hardware) RAKE fingers. On the input side, each of the RAKE fingers has a random access memory RAM1-8, downstream of which there is a time-variant interpolator TVI1-8 and, as the signal path continues, a multiplier M1-8, an integrate and dump unit ID1-8 and the already mentioned weighting unit WG. The integrate and dump

units ID1-8 may each be bridged via switches S1-8, respectively. As illustrated in Fig. 2 and as will be explained in more detail later, the weighting unit WG may optionally have a multiplexer MUX connected upstream of it, and a demultiplexer DMUX connected downstream of it.

The method of operation of the RAKE finger section RF is now described.

First, let us consider the reception of a signal, which has been transmitted from a single subscriber, in the FDD mode. The fundamental principle of RAKE receivers, which is known per se, contains each RAKE finger being associated with one, and only one, path (subchannel) through the air interface. Therefore, the received data items $\underline{r}_{P1}$, $\underline{r}_{P2}$ and $\underline{r}_{P8}$ which are passed to the inputs of the individual RAKE fingers represent different versions of one and the same transmitted signal, which have reached the receiver via different propagation paths P1, P2, ..., P8 through the air interface.

The subdivision of the sample values (data $\underline{r}$ into the individual path components $\underline{r}_{P1}$, $\underline{r}_{P2}$, ..., $\underline{r}_{P8}$ is carried out under the control of the search and synchronization unit SE using the path information ADD_P. ADD_P indicates address areas in the input memory IN_RAM in which sample values relating to the same transmission path are stored, and therefore sample

values are read on a path-related basis from the input memory IN_RAM, and the corresponding data items $\underline{r}_{P1}$, $\underline{r}_{P2}$, ..., $\underline{r}_{P8}$ are passed to the individual RAKE fingers. The path information ADD_P is also passed to the channel estimator CE.

The synchronization information Sync that is emitted from the search and synchronization unit SE contains signals "to" and "μ" for each RAKE finger. The signals to represent individual time-controlled read instructions for the memory RAM1-8, and result in rough synchronization of the individual RAKE fingers to an accuracy of T_c.

The fine synchronization is carried out by the interpolators TVI1-8 by interpolation of the sample values in the respective RAKE fingers as a function of the individual interpolation signals μ. The interpolation signals μ are determined, for example by an early/late correlator, in the search and synchronization unit SE.

The interpolation of the sample values allows the sampling rate in each RAKE finger to be reduced to $1/T_c$, that is to say each chip is represented by one signal value. The signals downstream of the interpolators TVI1-8 are synchronized with an accuracy of at least $T_c/2$.

In summary, the memory RAM1-8 and the interpolators TVI1-8 provide compensation for the different path delay times of a subscriber signal which is subject to multipath propagation.

By way of example, MF equalization is carried out in the FDD mode. For this purpose, the signals which are produced on the output side of the interpolators TVI1-8 are first despread by multipliers M1-8 (spreading code: C_{sp}) and are descrambled (scrambling code: C_{sc}). This is done by direct, chip-by-chip multiplication of these two code sequences onto the signals (which are likewise at the chip clock rate).

The switches S1-S8 are open. The despread and descrambled data signals are accumulated over a symbol time period T_S by the integrate and dump units ID1, ID2,...ID8. The accumulation results in the signal rate in each RAKE finger being reduced to the value $1/T_S$.

The symbol time period T_S is dependent on the spreading factor Q of the spreading code C_{SP} that is used. The spreading factor Q indicates the number of chips per data symbol, that is to say $Q = T_S/T_C$. In the FDD mode for UMTS, Q may assume values of between 2 and 512.

The path-related data symbols, which are now at the symbol clockrate, are multiplied by multipliers MUL1, MUL2, ...,

MUL16 in the weighting unit WG by the corresponding MF equalizer coefficients which are emitted at the symbol clock rate from the calculation unit CU. In the process, each data symbol is multiplied by one equalizer coefficient.

The number of multipliers MUL1-16 should be chosen such that sufficient multiplication capacity is available even for a low spreading factor Q. 16 multipliers MUL1-16 are used in the present example. Since the multiplexing of the RAKE fingers results in their effective number possibly being greater than the number of multipliers MUL1-16 (as will be explained in the following text), the signals from the individual RAKE fingers are distributed between the multipliers MUL1-16 via a multiplexer MUX as well as suitable buffer stores, which are not described here. The demultiplexer DMUX reverses the combining of the signals once again on the individual multipliers MUL1-16. Path-related signals are thus once again produced on the outputs of the demultiplexer DMUX.

The combiner CB has, for example, four accumulators AC1, AC2, AC3, AC4. Each individual accumulator AC1, AC2, AC3, AC4 operates as a maximum ratio combiner (MRC), that is to say it once again joins the path versions that are produced at the output of the RAKE finger section RF together to form a subscriber signal. If only a single subscriber signal is detected (that is to say in the FDD mode, where only signal

versions relating to this subscriber signal are processed in the RAKE receiver), only one accumulator is required, for example, AC1. The signal that has been combined in this way is temporarily stored in a buffer store BS, and forms the reconstructed, transmitted subscriber signal $\hat{\underline{s}}$.

The method of operation of the RAKE finger section RF for multiple subscriber equalization in the TDD mode differs from the method of operation as described above for the FDD mode by the sample values $\underline{r}$ being split between the individual RAKE fingers. In this case, the RAKE fingers are not associated with specific paths through the air interface and thus the RAKE fingers are not all synchronized on a path-specific basis either.

Instead of this, only a first RAKE finger is synchronized to one channel, and a fixed relative time offset of in each case one symbol time period, that is to say Q chips, is set between the remaining fingers. This is achieved, for example, by all the other RAKE fingers each accessing the data that is stored in the memories RAM1, RAM2, ..., RAM8 with a time offset $T_c \cdot Q$ with respect to the previous finger. These data items are identical, which results in that the data stored in the memories RAM1, RAM2, ..., RAM8 in each case contains the sample values $\underline{r}$.

A further difference from the FDD mode is that, as already mentioned, JD equalization is carried out in the TDD mode. The major difference between the TDD mode and the FDD mode is that the weighting unit WG operates at the chip clock rate, that is to say the calculation unit CU calculates the equalizer coefficients chip-by-chip, and the weighting unit WG multiples these chip-by-chip onto the signals in the RAKE fingers. The despreading and descrambling of the received signals are carried out during the equalization process in the TDD mode.

As a consequence of this, no despreading/descrambling of the signals is carried out by the multipliers M1-8 in the TDD mode, and the integrate and dump units ID1-8 are bridged by closing the switches S1-8 in the TDD mode. This results in the output signals from the interpolators TVI1-8 still being at the chip clockrate $1/T_c$ at the input to the multiplexer MUX.

The components of the detected subscriber signals are joined together by accumulators AC1-4 in the signal path downstream of the weighting unit WG. In this case as well, each accumulator AC1-4 is associated with one subscriber signal or channel and carries out an MRC operation with respect to this - as in the FDD mode. However, in the TDD mode, each

accumulator AC1-4 also operates as an integrate and dump unit, that is to say reduces the signal clock rate from the chip clock rate to the symbol clock rate.

In contrast to the possible signal rates (chip rate or symbol rate), the processing frequencies that are used in the respective units may each differ for both modes. This is done in particular by what hardware functional units in the RAKE receiver are multiplexed and are thus used "more than once". This will be explained in the following text with reference to a configuration suitable for multimode operation of the RAKE structure illustrated in Figs. 1 and 2.

This is based on the assumption of the baseband section of the RAKE receiver, as illustrated in Fig. 2, containing 8 hardware RAKE fingers, 16 hardware multipliers MUL1-16 and four hardware accumulators AC1-4. Another assumption is quadruple multiplexing (not illustrated) of each (hardware) RAKE finger, so that 32 RAKE fingers (8 actual fingers and 24 virtual fingers) are effectively available. Furthermore, each RAKE finger is formed on a two-channel basis (in a manner which is likewise not illustrated) since, as already explained, I and Q components of the data items $\underline{r}_{P1}$, $\underline{r}_{P2}$, ..., $\underline{r}_{P8}$ must in each case be processed. If it is also remembered that a complex multiplication operation contains four real multiplication operations, the number of multiplication operations to be

carried out in the two modes by the multipliers MUL1-16 in the weighting unit WG is now described.

FDD mode: 256 real multiplication operations (4 real multiplication operations × 2 components × 32 fingers) must be carried out per symbol time period $T_S = Q \cdot T_c$; since a maximum signal rate of $1/T_S = 1/(2 \cdot T_c) = 2.048$ MHz results for $Q = 2$, a total of 256 real multiplication operations must be carried out within $T_S = 488$ ns in the worst case ($Q = 2$). If there are 16 multipliers MUL1-16, a multiplication must then be completed at the latest after 30.51 ns. This condition is satisfied for a processing frequency of 32 MHz.

TDD mode: 64 complex multiplication operations, that is to say 256 real multiplication operations, must be carried out per chip time period T_c; 256 multiplication operations must therefore be carried out in 244 ns with a chip rate of $1/T_c = 4.096$ MHz. Since, in consequence, a multiplication operation must be completed at the latest after 15.25 ns when there are 16 multipliers, the multiplication field MUL1-16 must be clocked at a processing frequency of 64 MHz.

Therefore, the processing frequency required for the weighting unit WG in the FDD mode is dependent on the spreading factor Q and is 32 MHz/Q. Subject to the stated preconditions, it is

always 64 MHz in the TDD mode, irrespective of the spreading factor Q.

Fig. 3 shows the combiner CB in greater detail. As can be seen from Fig. 3, each complex accumulator AC1-4 is configured to accumulate the I and Q signal components for two channels. As already mentioned, each complex accumulator AC1-4 is associated with one, and only one, physical channel, for example the DPCH (Dedicated Physical Control Channel). Each accumulator AC1-4 contains an enable unit FE, an adder SU, a demultiplexer DM, two buffer stores PM1, PM2 and a multiplexer MU, whose output is passed to the enable unit FE.

p_i denotes the total number of available (actual and multiplexed) RAKE fingers which are associated with an i-th physical channel. The number p_i corresponds to the number of detected paths for the channel. The spreading factor that is used in this channel is denoted Q_i (the spreading factors that are used in the channels may differ).

At the input of the accumulator ACi, i = 1, ..., 4, which is associated with the i-th physical channel, a data rate $R_i = p_i/(Q_i \cdot T_c)$ which is related to this channel occurs in the FDD mode, that is to say p_i times the symbol rate (since p_i equalized data symbols must be combined per symbol time period). In the TDD mode, the channel-related data rate R_i at

the input of an accumulator is always p_i/T_c (p_i equalized chips must be combined per chip time period).

In the FDD mode, the channel-related data rate at the output of the accumulator is ACi $1/(Q_i \cdot T_c) = 1/T_s$, since p_i incoming data symbols are combined to form one data symbol. The combined data symbols are emitted unchanged at the symbol clock rate.

In the TDD mode, the signal clock rate is converted to the symbol clock rate by accumulation of the individual chips over one symbol time period. The accumulators AC1-4 are thus used not only for a combination of the signals from different RAKE fingers but, furthermore, also act as an integrate and dump unit in the TDD mode. In the TDD mode, the channel-related data rate at the output of the accumulator is also $1/(Q_i \cdot T_c) = 1/T_s$.

The use of a RAKE receiver structure for carrying out JD equalization is based on the fact that the system matrix of a JD transmission system can be mapped onto the system matrix of a RAKE receiver which is oversampled Q times. This will now be explained in detail.

A transmission channel from the k-th subscriber is described by a matrix $\underline{A}_G^{(k)}$ of dimension $W_s \cdot Q \times (L_s+W_s-1)$ in the chip clock channel model, represented in the matrix vector form, and this describes both the transmitter-end signal processing by multiplication of spreading codes and scrambling codes onto the data symbols $\underline{s}$ to be transmitted, and the signal distortion which is suffered during transmission via the air interface. L_s denotes the channel length in symbols, that is to say the number of symbols taken into account for the channel memory, and W_s denotes the (selectable) number of symbols taken into account for the equalization process. In a corresponding manner, L denotes the channel length in chips on the basis of the chip clock channel model, and W denotes the number of chips taken into account for the equalization process (length of the equalizer in chips). Thus, L_s = ceil{L/Q} and W_s = ceil{W/Q}, where ceil {·} is rounded to the next higher integer number. A superscript T denotes the transposed vector or the transposed matrix, and underscores indicate that a variable is a complex value.

A sequence containing L_s+W_s-1 data symbols $\left\{\underline{s}_{n-L_s+1}^k,\ldots,\underline{s}_n^k,\ldots,\underline{s}_{n+W_s-1}^k\right\}$ to be transmitted for the k-th subscribed is described in the vector matrix form by the (column) vector $\underline{s}_n^{(k)} = (\underline{s}_{n-L_s+1}^k \cdots \underline{s}_{n+W_s-1}^k)^T$ of dimension $(L_s+W_s-1)\times 1$ relating to the n-th time step.

With regard to all K subscribers, the so-called "combined" vector of all the transmitted data symbols, relating to the n-th time step, is formed using

$$\underline{s}_n = \left(\underline{s}_n^{(1)T} \ldots \underline{s}_n^{(k)T} \ldots \underline{s}_n^{(K)T}\right)^T \qquad (1)$$

The "combined" vector has the dimension $K \cdot (L_s+W_s-1) \times 1$.

The transmitted data symbols are spread-coded, are each transmitted via two or more paths to the receiver, and are equalized there by joint detection (JD).

The equation for the reconstruction $\hat{\underline{s}}_n^k$ of the data symbol that is transmitted by the k-th subscriber with respect to the time step n is, in the receiver, as follows:

$$\hat{\underline{s}}_n^k = \underline{m}^{(k)} \underline{r}_n$$

where $\underline{r}_n = \underline{A}_G \underline{s}_n \qquad (2)$

In this case, the entire multiple subscriber system containing K subscribers (including spread coding and signal distortion which occurs during signal transmission) is described by the so-called multiple subscriber system matrix $\underline{A}_G$ of dimension $W_s \cdot Q \times K(L_s+W_s-1)$.

The vector $\underline{r}_n$ represents the received data at the chip clock rate. The receiver-end JD equalization of the received data from the k-th subscriber is in this model provided by an equalizer vector $\underline{m}^{(k)}$ of dimension $1 \times W_s \cdot Q$, which is calculated on the basis of the estimated channel coefficients by the calculation unit CU. The $W_s \cdot Q$ elements of the equalizer vector $\underline{m}^{(k)}$ are the equalizer coefficients for the k-th subscriber. The calculation rule for the equalizer vector $\underline{m}^{(k)}$ is dependent on the chosen equalizer algorithm. This will be described later for the case of ZF equalization.

The multiple subscriber system matrix $\underline{A}_G$ is obtained in the following manner from system matrices $\underline{A}_G^{(k)}$ of dimension $W_s \cdot Q \times (L_s + W_s - 1)$ for the individual subscribers:

$$\underline{A}_G = \left[\underline{A}_G^{(1)} \underline{A}_G^{(2)} \ldots \underline{A}_G^{(K)}\right] \qquad (3)$$

The subscriber system matrices $\underline{A}_G^{(k)}$ are defined by:

$$\underline{A}_G^{(k)} = \begin{bmatrix} \left[\underline{A}'^{(k)}\right] 0 \ldots\ldots 0 \\ 0 \left[\underline{A}'^{(k)}\right] 0 \ldots 0 \\ 00 \left[\underline{A}'^{(k)}\right] 0 \ldots 0 \\ 0 \ldots\ldots 0 \left[\underline{A}'^{(k)}\right] \end{bmatrix} \qquad (4)$$

where $\underline{A}^{'(k)}$ in the general case is a matrix of dimension $Q \times L_s$ which is quoted here, in order to improve the representation, for the special case of $L_s = 2$ (that is to say the dimension $Q \times 2$).

$$\underline{A}^{'(k)} = \begin{bmatrix} \underline{a}_{Q+1}^{(k)} & \underline{a}_{1}^{(k)} \\ \underline{a}_{Q+2}^{(k)} & \underline{a}_{2}^{(k)} \\ \vdots & \vdots \\ \underline{a}_{Q+L-1}^{(k)} & \underline{a}_{L-1}^{(k)} \\ 0 & \underline{a}_{L}^{(k)} \\ \vdots & \vdots \\ 0 & \underline{a}_{Q}^{(k)} \end{bmatrix} \qquad (5)$$

The elements in the matrix $\underline{A}^{'(k)}$ are obtained from the respectively used spreading codes and channel characteristics:

$$\underline{a}^{(k)} = \underline{C}^{'(k)} \underline{h}^{(k)T} \qquad (6)$$

In this case, $\underline{a}^{(k)} = \left(\underline{a}_1^{(k)} \ldots \underline{a}_{Q+L-1}^{(k)}\right)^T$ is a vector of dimension $(Q+L-1) \times 1$ and $\underline{C}^{'(k)}$ is a matrix which is produced by the spreading code C_{sp} for the k-th subscriber under consideration, in this case denoted $\underline{c}^{(k)} = \left(\underline{c}_1^k \ldots \underline{c}_Q^k\right)$

$$C'^{(k)} = \begin{bmatrix} \underline{c}_1^k & 0 & \cdots & 0 \\ \underline{c}_2^k & \underline{c}_1^k & & \vdots \\ \vdots & \underline{c}_2^k & & \\ \underline{c}_Q^k & & & \vdots \\ 0 & \underline{c}_Q^k & & 0 \\ \vdots & \cdot & & \underline{c}_1^k \\ & & \cdot & \underline{c}_2^k \\ \vdots & & & \vdots \\ 0 & \cdots & 0 & \underline{c}_Q^k \end{bmatrix} \qquad (7)$$

of dimension (Q+L-1)×L.

$\underline{h}^{(k)} = \left(\underline{h}_1^k \ldots \underline{h}_L^k\right)^T$ is the (column) vector which is formed from the channel impulse response $\underline{h}_1^k$, $\underline{h}_2^k$, ..., $\underline{h}_L^k$ of length L for the k-th subscriber (as already mentioned, L denotes the channel length (channel memory) in chips).

To simplify the representation, it is assumed that no scrambling code is used.

An analogous description of a transmission system (but relating to block-by-block data transmission) is known from the prior art and is described in detail on pages 188-215 of the book titled "Analyse und Entwurf digitaler Mobilfunksysteme" [Analysis and Design of Digital Mobile Radio Systems] by P. Jung, B.G. Teubner Verlag Stuttgart, 1997. This

literature reference is incorporated by reference into the subject matter of the present document.

As is obvious, the "equalizer" $\underline{m}^{(k)}$ which is required to calculate a transmitted data symbol from the k-th subscriber contains Q "sub-equalizers" of length W_s. Therefore, a RAKE receiver operated with Q-times oversampling is required for JD equalization. It is also obvious from the above analysis that the despreading is an integral component of the equalization process.

In the case of ZF equalization, the equalizer coefficients (that is to say the elements of the equalizer vector $\underline{m}^{(k)}$) are calculated by solving the equation system:

$$\underline{m}^{(k)}\underline{A}_G = \zeta_j \qquad (8)$$

In this case, ζ_j is a $1\times K\cdot(L_s+W_s-1)$ (row) vector, which predetermines the ZF condition for a specific (k-th) subscriber. The ZF vector ζ_j can be represented as follows:

$$\zeta_j = (0\ldots010\ldots0) \qquad (9)$$

with the 1 in the j-th position representing

$$j = (k-1)\ (L_s+W_s-1)+1,\ \ldots,\ k(L_s+W_s-1).$$

Fig. 4 shows the calculation of $\hat{\underline{s}}_n^k$ for Q = 4, W_s = 3, L_s = 3 (L and W are 11 in this case) and K = 1 by the RAKE receiver on the basis of a representation of a detail of the system matrix $\underline{A}_G$, the equalizer coefficients m1 to m12, the data items $\underline{s}_{n-2}$ to $\underline{s}_{n+2}$ transmitted (by the one subscriber) (at the symbol rate), the received data items r1 to r12 (at the chiprate) and the data symbol $\hat{\underline{s}}_n$ estimated for the n-th time step (underscores are ignored). One and only one finger, which is oversampled Q times, of the RAKE receiver is used for every Q chips. The RAKE finger #1 processes the first received Q chips, the RAKE finger #2 processes the second Q chips delayed by Q chips, etc. Therefore, the input signal to each RAKE finger is a signal that has been oversampled Q times. Each sample value contains the same information with regard to the transmitted data symbol, but different information with regard to the spreading code used (and the scrambling code if appropriate) and the transmission channel.

ZF equalization and a possible method for solving the equation 8 are described in detail in Published, Non-Prosecuted German Patent Application DE 101 06 391 A1, which is hereby incorporated by reference herein.